CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A semiconductor wafer comprising:

a semiconducting or non-semiconducting substrate;

a buried insulator layer located on an upper surface of the substrate;

an intermediate adhesion layer located on an upper surface the buried insulator layer; and

a Ge-containing layer located on an upper surface of the intermediate adhesion layer, wherein said Ge-containing layer is attached to the buried insulator layer by the intermediate adhesion layer.

2. The semiconductor wafer of Claim 1 wherein a surface of the Ge-containing layer that is in contact with the intermediate adhesion layer is roughened.

3. The semiconductor wafer of Claim 1 wherein said substrate is a semiconducting substrate which comprises a semiconductor selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge, GaAs, InAs, InP and other III/V or II/VI compound semiconductors.

4. The semiconductor wafer of Claim 1 wherein said substrate is a Si-containing semiconductor substrate selected from the group consisting of Si, SiGe, SiC, SiGeC, Si/Si, Si/SiC, Si/SiGeC and preformed silicon-on-insulators.

5. The semiconductor wafer of Claim 1 wherein said substrate comprises strained layers, unstrained layers or a combination thereof.

6. The semiconductor wafer of Claim 1 wherein said buried insulator layer is a crystalline or non-crystalline oxide, nitride or combination thereof.

7. The semiconductor wafer of Claim 1 wherein said buried insulator layer comprises $SiO_2$.

8. The semiconductor wafer of Claim 1 further comprising a buried diffusive mirror located in between the buried insulator layer and another buried insulator.

9. The semiconductor wafer of Claim 8 wherein the buried diffusive mirror is corrugated.

10. The semiconductor wafer of Claim 9 wherein the buried diffusive mirror comprises a metal.

11. The semiconductor wafer of Claim 1 wherein said intermediate adhesion layer is a Si material.

12. The semiconductor wafer of Claim 11 wherein said Si material is single crystal Si, polycrystalline Si, amorphous Si, epitaxial Si or combinations and multilayers thereof.

13. The semiconductor wafer of Claim 1 wherein said Ge-containing layer is a pure Ge layer.

14. The semiconductor wafer of Claim 1 wherein said Ge-containing layer is a thin layer having a thickness from about 1 nm to about 1000 nm.

15. A semiconductor wafer comprising:
a substrate;

a Bragg mirror located on said substrate; and

a Ge-on-insulator film located on said Bragg mirror, wherein said Bragg mirror comprises a plurality of two alternating dielectric films.

16. The semiconductor wafer of Claim 15 wherein said Bragg mirror comprises a plurality of alternating layers of $SiO_2$ and $Si_3N_4$.

17. A semiconductor wafer comprising

a semiconducting or non-semiconducting substrate;

a buried insulator layer located on an upper surface of the substrate; and

a Ge-containing layer located on an upper surface of the buried insulator layer, wherein said Ge-containing layer is attached to the buried insulator film by a roughened surface.

18. The semiconductor wafer of Claim 17 wherein said substrate is a semiconducting substrate which comprises a semiconductor selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge, GaAs, InAs, InP and other III/V or II/VI compound semiconductors.

19. The semiconductor wafer of Claim 17 wherein said substrate is a Si-containing semiconductor substrate selected from the group consisting of Si, SiGe, SiC, SiGeC, Si/Si, Si/SiC, Si/SiGeC and preformed silicon-on-insulators.

20. The semiconductor wafer of Claim 17 wherein said substrate comprises strained layers, unstrained layers or a combination thereof.

21. The semiconductor wafer of Claim 17 wherein said buried insulator layer is a crystalline or non-crystalline oxide, nitride or combination thereof.

22. The semiconductor wafer of Claim 17 wherein said buried insulator layer comprises $SiO_2$.

23. The semiconductor wafer of Claim 17 wherein said buried insulator layer is a Bragg mirror having at least a pair of alternating dielectric layers of different refractive indices.

24. The semiconductor wafer of Claim 17 further comprising a buried diffusive mirror located in between the buried insulator layer and another buried insulator.

25. The semiconductor wafer of Claim 24 wherein the buried diffusive mirror is corrugated.

26. The semiconductor wafer of Claim 25 wherein the buried diffusive mirror comprises a metal.

27. The semiconductor wafer of Claim 17 wherein said Ge-containing layer is a pure Ge layer.

28. The semiconductor wafer of Claim 17 wherein said Ge-containing layer is a thin layer having a thickness from about 1 nm to about 1000 nm.

29. A semiconductor structure comprising at least the semiconductor wafer of Claim 1 and at least one device or circuit located thereon.

30. The semiconductor structure of Claim 29 wherein the device is a Ge-photodetector.

31. The semiconductor structure of Claim 29 wherein the circuit is a Si-containing circuit.

32. The semiconductor structure of Claim 29 wherein said device or said circuit is monolithically integrated.

33. A semiconductor structure comprising at least the semiconductor wafer of Claim 17 and at least one device or circuit located thereon.

34. The semiconductor structure of Claim 33 wherein the device is a Ge-photodetector.

35. The semiconductor structure of Claim 33 wherein the circuit is a Si-containing circuit.

36. The semiconductor structure of Claim 33 wherein said device or said circuit is monolithically integrated.

37. A method for forming a germanium-on-insulator comprising:

forming an intermediate adhesion layer on a surface of a Ge-containing donor substrate;

forming a buried insulator layer on said intermediate adhesion layer;

implanting hydrogen into said Ge-containing donor substrate; and

bonding an exposed surface of the buried insulator layer to a semiconducting or non-semiconducting substrate, wherein during said bonding a portion of the Ge-containing donor substrate is transferred to said substrate.

38. The method of Claim 37 wherein a surface of the Ge-containing donor substrate is roughened prior to said forming said intermediate adhesion layer.

39. The method of Claim 38 wherein said roughened surface is achieved by sputtering in an inert gas.

40. The method of Claim 37 wherein the Ge-containing donor substrate is a pure Ge wafer.

41. The method of Claim 37 wherein the implanting is performed using a hydrogen dose from about 1E15 $cm^{-2}$ to about 1E17 $cm^{-2}$.

42. The method of Claim 41 wherein the implanting is performed using a hydrogen dose from about 3E16 to about 4E16 $cm^{-2}$.

43. The method of Claim 37 wherein the implanting is performed at an implant temperature from about 20°C to about 40°C.

44. The method of Claim 37 wherein the exposed surface of the buried insulating and the substrate are cleaned and surface treated prior to bonding.

45. The method of Claim 37 wherein said bonding comprises wafer flipping, contact bonding and annealing.

46. The method of Claim 45 wherein said annealing comprises a first anneal at first temperature that is capable of enhancing bonding between the substrate and the buried insulator layer; a second anneal at a second temperature that is capable of said removing a portion of the Ge-containing donor layer; and a third anneal at a third temperature that is capable of further strengthening bonding.

47. The method of Claim 46 wherein the first temperature of said first anneal is from about 100°C to about 300°C for a time period from about 1 hour to about 48 hours.

48. The method of Claim 46 wherein the second temperature of the second anneal is from about 250°C to about 400°C for a time period from about 1 hour to about 24 hours.

49. The method of Claim 46 wherein the third temperature of the third anneal is from about 500°C to about 900°C for a time period from about 1 hour to about 48 hours.

50. The method of Claim 46 wherein the first, second and third anneals are performed in the same or different inert gas ambient that may optionally be diluted with an oxygen-containing gas.

51. The method of Claim 46 wherein the first, second and third anneals are carried out using a single ramp-up rate or using various ramp and soak cycles.

52. The method of Claim 37 further comprising performing a chemical mechanical polishing step between said forming the buried insulator layer and said implanting hydrogen.

53. A method for forming a germanium-on-insulator comprising:

roughening a surface of a Ge-containing donor substrate;

forming a buried insulator layer on said roughening surface;

implanting hydrogen into said Ge-containing donor substrate; and

bonding an exposed surface of the buried insulator layer to a semiconducting or non-semiconducting substrate, wherein during said bonding a portion of the Ge-containing donor substrate is transferred to said substrate.

54. The method of Claim 53 wherein an intermediate adhesion layer is formed on the roughened surface and said buried insulator is formed on said intermediate adhesion layer.

55. The method of Claim 53 wherein said roughened surface is achieved by sputtering in an inert gas.

56. The method of Claim 53 wherein the Ge-containing donor substrate is a pure Ge wafer.

57. The method of Claim 53 wherein the implanting is performed using a hydrogen dose from about 1E15 $cm^{-2}$ to about 1E17 $cm^{-2}$.

58. The method of Claim 53 wherein the implanting is performed using a hydrogen from about 3E16 $cm^{-2}$ to about 4E16 $cm^{-2}$.

59. The method of Claim 53 wherein the implanting is performed at an implant temperature from about 20°C to about 40°C.

60. The method of Claim 53 wherein the exposed surface of the buried insulating and the substrate are cleaned and surface treated prior to bonding.

61. The method of Claim 53 wherein said bonding comprises wafer flipping, contact bonding and annealing.

62. The method of Claim 61 wherein said annealing comprises a first anneal at first temperature that is capable of enhancing bonding between the substrate and the buried insulator layer; a second anneal at a second temperature that is capable of said removing a portion of the Ge-containing donor layer; and a third anneal at a third temperature that is capable of further strengthening bonding.

63. The method of Claim 62 wherein the first temperature of said first anneal is from about 100°C to about 300°C for a time period from about 1 hour to about 48 hours.

64. The method of Claim 62 wherein the second temperature of the second anneal is from about 250°C to about 400°C for a time period from about 1 hour to about 48 hours.

65. The method of Claim 62 wherein the third temperature of the third anneal is from about 500°C to about 900°C for a time period from about 1 hour to about 48 hours.

66. The method of Claim 62 wherein the first, second and third anneals are performed in the same or different inert gas ambient that may optionally be diluted with an oxygen-containing gas.

67. The method of Claim 62 wherein the first, second and third anneals are carried out using a single ramp-up rate or using various ramp and soak cycles.

68. A method of forming a semiconductor wafer comprising:

providing a substrate that includes a buried insulator, a Si adhesion layer located on the buried insulator, and Ge-containing layer on the Si adhesion layer;

annealing the substrate to cause thermal mixing of the Ge-containing layer and the Si adhesion layer to form a SiGe-on-insulator or a Ge-on-insulator.